



Attorney Docket No. 21.1978C

C. J. Staas

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Hideo Akiyoshi

Application No.: 10/056,072

ATTENTION

Confirmation No.: 3156

CERTIFICATE OF CORRECTION

Filed: March 26, 2002

BRANCH

U.S. Patent No.: 6,975,151

Batch No.:

Issued: December 13, 2005

For: LATCH CIRCUIT HAVING REDUCED INPUT/OUTPUT LOAD, MEMORY AND SEMICONDUCTOR CHIP

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Certificate
MAY 10 2006
of Correction

Sir:

Patentee(s) respectfully request(s) that a Certificate of Correction be issued in the subject patent, pursuant to 35 USC § 254 and 37 CFR § 1.322, to correct the error(s) shown on the attached Form PTO-1050. A check in the amount of \$100 to cover the cost of the Certificate is attached.

One or more of the errors shown on the attached Form PTO-1050 is or are within the responsibility of the undersigned; each thereof is of a clerical or typographical nature or of minor character and occurred in good faith, and the correction thereof is consistent with the prosecution record.

Respectfully submitted,

STAAS & HALSEY LLP

Date:

May 1, 2006

By:

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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO : 6,975,151

DATED : December 13, 2005

INVENTOR(S) : Hideo Akiyoshi

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

On the cover page, in the title (54), after "LOAD", insert --,--.

Column 1, in the title, "LOAD", insert --,--.

Column 12, line 17, change "inverted" to --inverter--.

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PATENT NO. 6,975,151

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